Patent Claims

1. Process for forming a housing for electronic modules, in particular sensors, integrated circuits and optoelectronic components;
comprising the steps of:
- providing a substrate (1), of which at least a first substrate side (1a) is to be encapsulated,
- providing a vapor-deposition glass source (20),
- arranging the first substrate side (1a) in such a manner with respect to the vapor-deposition glass source that the first substrate side (1a) can be vapor-coated;
- vapor-coating the first substrate side with a glass layer (4).

2. The process as claimed in claim 1, wherein the substrate provided has one or more regions comprising semiconductor structures (2) and comprising connection structures or for forming semiconductor structures (2) and connection structures (3).

3. The process as claimed in claim 2, wherein the one or more regions having semiconductor structures (2) are arranged on the first side (1a) of the substrate.

4. The process as claimed in claim 3, wherein the substrate is provided with a passivation layer (10, 11) on a second side (1b), which is on the opposite side from the first side (1a).

5. The process as claimed in one of the preceding claims, the substrate comprising a wafer, wherein the process comprises the packaging of components which still form part of a wafer.

6. The process as claimed in one of the preceding claims, wherein the substrate (1) is vapor-coated with a glass layer (4, 10, 11) on two sides (1a, 1b).

7. The process as claimed in one of the preceding claims, wherein a vapor-deposition glass source (20) which generates at least a binary glass system is provided.

8. The process as claimed in one of the preceding claims, wherein the vapor-deposition glass source (20) is operated until the glass layer (4) has a thickness in the range from 0.01 to 1000 µm, in particular on the first substrate side.

9. The process as claimed in one of the preceding claims, wherein as part of the step of providing a vapor-deposition glass source (20), a reservoir comprising organic constituents is provided, and these organic constituents are converted into the vapor state through application of a vacuum or through heating, so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the substrate side.

10. The process as claimed in one of the preceding claims, wherein the glass layer thickness is in the range between 0.1 and 50 µm.

11. The process as claimed in one of the preceding claims, wherein the glass layer thickness is in the range between 50 and 200 µm.

12. The process as claimed in one of the preceding claims, wherein the vapor-deposition glass of the source (20) is generated from a glass target (23) by means of electron beam

(24).

13. The process as claimed in one of the preceding claims, wherein the vapor-deposition glass used is a borosilicate glass containing aluminum oxide and alkali metal oxide fractions.

14. The process as claimed in one of the preceding claims, wherein the vapor-deposition glass has a coefficient of thermal expansion which is virtually equal to that of the substrate.

15. The process as claimed in one of the preceding claims, wherein the glass layer (4) is produced with a thickness which is required for a hermetic seal, and wherein a layer of plastic (5) is applied above the glass layer (4) in order to facilitate further processing of the substrate (1).

16. The process as claimed in one of the preceding claims, wherein a plurality of glass layers are vapor-deposited onto the substrate (1), it being possible for the glass layers to consist of various glass compositions.

17. The process as claimed in one of the preceding claims, wherein the further processing of the substrate (1) involves the removal of material from a second substrate side (1b), which is on the opposite side from the first substrate side (1a).

18. The process as claimed in one of the preceding claims, wherein the substrate (1) includes a wafer having a plurality of semiconductor structures (2) and connection structures (3), with the second substrate side (1b), which is on the opposite side from the first substrate side (1a), being thinned, pits (6) being etched on the second substrate side

(1b) in the region of the connection structures to be produced, the regions for forming the semiconductor structures (2) being lithographed using plastic layers, line contacts (7) being produced on the second substrate side (1b) in the regions having connection structures (3), the plastic being removed from the second substrate side (1b), a ball grid array (8) being applied at the line contacts (7), and
the wafer being divided up so as to form a plurality of electronic modules which each have first, encapsulated sides (1a).

19. The process as claimed in claim 18, wherein the second substrate side (1b) is provided with a plastic covering (10) while leaving clear the ball grid regions (8).

20. The process as claimed in claim 18 or 19, wherein after the plastic has been removed from the second substrate side (1b) the whole of the second substrate side is vapor-coated with a glass layer (11), and wherein the line contacts (7) are uncovered by local elimination of the glass layer (11), after which the steps of applying the ball grid array (8) and of dividing up the wafer are carried out in order to obtain electronic modules which are encapsulated on both sides.

21. The process as claimed in claim 20, wherein the entire second substrate side is vapor-coated with a glass layer (11) with a thickness in the range from 1 to 50 µm, and

22. The process as claimed in one of claims 18 to 21, wherein the etching pits (6) which lead to the connection structures (3) are filled with conductive material (12), after which, with or without removal of the plastic (10) from the second substrate side (1b) and with or without a glass

layer (11) on the second substrate side (1b), and leaving clear the line contacts (7), the ball grid array (8) is applied at the line contacts (7) and/or at the filling material.

23. The process as claimed in one of the preceding claims, wherein the vapor-coating of the first substrate side (1a) with a glass layer (4) comprises plasma ion assisted deposition (PIAD).

24. An electronic module, in particular as a sensor or as an integrated circuit or as an optoelectronic component, producible by the process as claimed in one of the preceding claims.

25. The electronic module as claimed in claim 24, which on a first side (1a) has one or more regions with semiconductor structures (2), and connection structures (3), wherein the substrate is coated with a vapor-deposited glass layer (4) on at least one side.

26. The electronic module as claimed in claim 25, wherein a plastic layer (5) which reinforces the module is applied to the glass layer (4).

27. The electronic module as claimed in one of claims 25 or 26, wherein the substrate is thinned.

28. The electronic module as claimed in one of claims 25 to 27, wherein the substrate is provided with a passivation layer (10, 11) on a second side (1b), which is on the opposite side from a first side (1a) having semiconductor structures and connection structures.

29. The electronic module as claimed in one of claims 25 to 28, wherein the glass layer (4) comprises a mixed layer of inorganic and organic constituents.

30. The electronic module as claimed in one of claims 25 to 29, which includes a multilayer glass layer (4).

31. The electronic module as claimed in claim 30, wherein the individual layers of the glass layer have different compositions.

32. The electronic module as claimed in one of claims 25 to 31, wherein the substrate (1), on a second side (1b), has line contacts that are connected to connection structures on the first side (1a).

33. The electronic module as claimed in claim 32, which includes a ball grid array (8) at the line contacts.